INTEGRATED CIRCUIT CLOCK DISTRIBUTION

The present invention relates to semiconductor circuits and clock distribution to different areas of an integrated circuit. The invention is also concerned with clocking strategies to optimize a clock equilibrium among blocks for which inter-blocks synchronization is necessary.

5   In large-scale integrated circuits (ICs), the tendency is to an increase in the chip area and the clock frequency. ICs are built with elements like flip-flop cells whose operations and switching keep getting faster and the number of points to be balanced increases exponentially with the size of the chip. A consequence of these two trends is a worsening of the clock skew and the industry strives to maintain the quality of the overall clock tree of new circuit designs

10   to an acceptable level. Solutions have thus been contemplated to shorten clock skews however designers need to pay special attention to the power consumption which may tend to go up with some of the developed techniques.

US2002/0060595 discloses a method for decreasing clock skews of large-scale integrated circuits. This document proposes a semiconductor IC which includes a plurality of

15   areas which operate with independent clocks and a phase separation element which differentiates the phase of one of the clocks from the phases of the other clocks and distributes the clocks to the areas, respectively. In the disclosed circuit, a phase separation element distributes a clock to a clock driver of each area. The phase separation element has an element which sets and distributes the phase of each clock so that start points of each

20   cycle of the clocks to be distributed to the areas, respectively, are at different timings for each of the areas. In this solution, the distribution of the clock to a given area still relies on the distribution paths from the phase separation element and these paths from the main clock generator or phase separation element to areas to be supplied may be become large as the number of points in circuits increases. The depth of the overall clock tree of the circuit may

25   become large and distribution paths thus become unreliable and subject to external noise issues.

The inventors have sought a solution for clock distribution to logic blocks that alleviates the flaws of existing designs.

A circuit is proposed that includes a plurality of interconnected logic blocks. A

30   reference clock generator generates a reference clock signal that is distributed to all logic

blocks. Each block includes at least one local clock generator generating a respective set of synchronized local clock signals. The generator produces the local clock signals from the reference clock signal and further provides them to respective elements of the logic block. The circuit is such that a set of local clock signals of a first block is phase shifted relative to a

5   set of local clock signals of another block.

The invention introduces clock generators in each block so that clock generation can be managed locally compared to a design where generation and distribution of clocks within blocks is centrally managed. Managing clocks locally permits to reduce the scale of the circuit to the block level and thus avoids problems with clock equilibration and clock skews

10   of large chip designs. Allowing local clocks to be independent from one block to another permits to reduce the clock skews and the over-all quality of the clock tree is thus increased. The phase shift introduced between some logic blocks of the circuit prevents all local clocks from switching simultaneously which is known to cause power drain. Indeed, if all local clocks in the circuit were phase-synchronous and synchronized with the reference clock, one

15   may observe, at the level of the reference clock, peaks of drain of power around clock edges. Such phenomenom requires strong on-chip power supply which is often associated with yield loss. The phase shift introduced in the invention thus smoothes these power peaks. Another advantage of one or more embodiments of the invention is to reduce the number of circuit points that need to be balanced.

20   These and other aspects of the invention will be apparent from and will be elucidated with reference to the embodiments described hereinafter. The present invention will now be described in more detail, by way of example, with reference to the accompanying drawings, wherein:

Fig.1 is a block diagram of an examplary embodiment of logic blocks in a circuit of

25   the invention;

Fig.2 is a timing diagram showing local clocks of logic blocks of Fig.1;

Fig.3 is a block diagram of another examplary embodiment of logic blocks in a circuit of the invention;

Fig.4 is a timing diagram of local clocks of logic blocks of Fig.3;

30   Fig.5 and Fig.6 are block diagrams of other examplary embodiments of logic blocks in a circuit of the invention; and,

Fig.7 is a timing diagram of local clocks of logic blocks of Fig.6.

The invention will be illustrated by means of several examplary embodiments of blocks of a circuit of the invention. A circuit of the invention may include one or more types

of pairs or groups of blocks such as the ones presented here or a combination of the like. However the blocks' designs presented here, the elements contained therein and the data paths between blocks as shown in Fig.3 and Fig.6 are only given for illustrated purposes and should not be used to limit the scope of the invention and the design of a circuit of the

5   invention. In the following description, clocks generated in blocks 100, 200 and 300 are respectively referenced by suffixes phi1, phi2 and phi3.

Fig.1 is a first block diagram of an examplary embodiment of a portion of a circuit of the invention comprising logic blocks 100 and 200. The circuit of the invention may be any type of Integrated Circuit such as an RF circuit or a processing circuit. In this embodiment,

10   block 100 includes, for example, clock generator unit 110, flip-flop cells 120 and 130 and combinatorial cells 140 between data output of cell 120 and data input of cell 130. Clock generator unit 110 produces local clock signals clk1_phi1 and clk2_phi1 from a reference clock Clk_ref received from a reference clock generator of a circuit of the invention, e.g. internal clock signals clk1_phi1 and clk2_phi1 may be obtained from clock division and

15   phase shifting of the received reference clock clk_ref. Clocks clk1_phi1 and clk2_phi1 are synchronized with reference clock clk_ref. The reference clock generator of circuit is not shown in Fig.1 and may be implemented as the instantiation of a Phase Locked-loop block. Block 200 is similar to block 100 and comprises similar elements: local clock generator unit 210 produced local clock signals clk2_phi2 and clk1_phi2 supplied to respective enable

20   inputs of flip-flop cells 220 and 230 via memory 240.

In this first embodiment, blocks 100 and 200 operate independently from each other and no data exchange takes place between the two blocks. There is therefore no need to synchronize both blocks. On the contrary, in this embodiment, a phase-shift is arbitrarily introduced between the set of clocks generated in block 100, i.e. clk1_phi1 and clk2_phi1

25   and the set of clocks generated in block 200, i.e. clk1_phi2 and clk2_phi2. Respective local clocks of blocks 100 and 200 are shown in timing diagram of Fig.2 and as can be seen, a phase-shift of one clock cycle of the reference clock clk_ref is introduced by clock generator units 110 and 210. In addition, a clock tree may be built for each independent block 100 and 200 and each block is independently balanced to ensure no margin between clock edges of

30   the internal clock signals. A result of this is that all local clock signals of each respective block are synchronized for synchronous internal operations of the elements in a given block.

Fig.2 is another examplary embodiment of a portion of a circuit of the invention. Blocks 100 and 200 in this embodiment communicate via data path 400. Data path 400 may be a one-way single data path. Data output of cell 130 is connected to data input of flip-flop

cell 250 of block 200. Enable input of cell 250 is triggered by clock clk3_phi2 generated by clock generator unit 210. As shown in Fig.4, each block 100 and 200 is internally balanced and internal clocks of block 100, i.e. clock signals clk1_phi1 and clk2_phi1 are thus synchronized with each other and further synchronized with reference clock clk_ref from

5   which they are derived. In a similar fashion, in block 200, clocks signals clk1_phi2, clk2_phi2 and clk3_phi 2 are also synchronized with each other and with the reference clock clk_ref from which they are also derived. In this embodiment, a phase shift of one reference clock cycle is also introduced between the set of internal clocks of block 100 and the set of internal clocks of block 200. Indeed, data is transmitted from cell 130 of block 100 to cell

10   250 of block 200 via data path 400. Data is applied onto data path 400 when enable input of cell 130 is activated, i.e. when clock signal clk1_phi of block 100 supplied to enable input of cell 130 toggles. Data is taken by cell 250 from data path 400 when enable input of cell 250 is activated, i.e. when clock signal clk3_phi2 of block 200 supplied to enable input of cell 250 toggles. In this examplary embodiment, clock signal clk3_phi2 toggles one clock cycle

15   later than internal clock clk1_phi1 of block 1 and current data is therefore present at data input of cell 250 when cell 250 is activated.

        In a fourth examplary embodiment depicted in Fig.5, switching of cell 250 is controlled by referenceclock clk_ref provided at the enable input of cell 250. However, because block 100 is internally balanced, the following two signals are synchronized with

20   each other:

        - clock signal clk1_phi which causes the activation of cell 130 and as a consequence the writing of data onto data path 400, and,

        - reference clock signal clk_ref.

In addition, cell 250 reads data path 400 when reference clock signal clk_ref toggles. A data

25   violation may then occur when cell 250 reads data from data path 400 which is not yert present and stable because it is simultaneoulsy outputed by cell 130. To this end, flip-flop cell 260 with an inverted enable input is placed onto data path 400 between cell 130 and cell 250 to permit reading of data on path 400 at the time of the down switching of the reference clock signal clk_ref. Data provided by cell 130 is therefore stable on data path 400 when cell

30   260 reads data conveyed on data path 400. Data may then be provided to cell 250 when reference clock clk_ref toggles up.

        Fig.6 proposes another embodiment of a portion of a circuit of the invention that includes blocks 100, 200 and 300. In this particular examplary embodiment of blocks 100, 200 and 300, a data bus 400 interconnects output of block 100 to input of blocks 200 and

300. Contrary to the embodiments presented in reference to Fig.3 and Fig.5 where data path 400 is a one-way data link, data bus 400 dues to its nature poses an additional constraint on the designs of blocks 100, 200 and 300. Indeed, data bus 400 may be a bidirectional communication bus and requires that data is written and read in a synchronous manner. Thus,

5   blocks 100, 200 and 300 need to be balanced with each other on top of their internal clock equilibrium. Clock generators 110, 210 and 310 are thus first set up to generate synchronized set of internal clocks within blocks 100, 200 and 300, i.e. the blocks are internally balanced. Then, a clock tree for the three blocks taken together is also equilibrated and all internal clocks are synchronized.

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